PATENT #16
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Appeal Brief filed 10/21/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re application of

Young-In PARK

Application No.: **09/855,694**

Filed: **May 16, 2001**

Confirmation No.: **9209**

Group Art Unit: **2823**

Examiner: **Julio J. Maldonado**

Customer No.: **30827**

For: **METHOD OF MANUFACTURING A THIN FILM TRANSISTOR AND MANUFACTURING EQUIPMENT**

APPELLANTS' BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to a Final Rejection of all pending claims that was mailed on December 4, 2002, and an Advisory Action that was mailed on March 25, 2003, and in support of a "Notice of Appeal" filed on April 4, 2003, Appellants hereby submit this Appeal Brief.

The fees required under § 1.17(f) and any required petition for extension of time for filing this brief and fees therefore are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief is transmitted in triplicate.

This brief contains items under the following headings as required by 37 C.F.R. § 1.192 and M.P.E.P. § 1206:

I. Real Party In Interest

II Related Appeals and Interferences

REAL PARTY IN INTEREST

The real party in interest for this appeal is: LG.Philips-LCD Co., Ltd.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Total Number of Claims in the Application

There are 20 claims pending in the application.

Current Status of Claims

Claims canceled: N/A

Claims withdrawn from consideration but not canceled: 6-14

Claims pending: 1-20

Claims allowed: N/A

Claims rejected: 1-5 and 15-20

Claims On Appeal: The claims on appeal are claims 1-20.

STATUS OF AMENDMENTS

The Examiner issued a Non-Final Rejection on June 19, 2002. Appellants amended the Specification to correct minor typographical errors, and amended FIG. 3 to include a "Related Art" legend in a Reply under 37 CFR § 1.111 on September 18, 2002. No claim amendments were made in the Reply filed on September 18, 2002. The Examiner issued a Final Rejection on December 4, 2002. Appellants filed a Response under 37 CFR § 1.116 on March 4, 2003. The claims were not amended after the final rejection. The Examiner responded to the Response under 37 CFR § 1.116 in an Advisory Action mailed March 25, 2003. In the Advisory Action, the Examiner indicated that Appellants' remarks in the Response under 37 CFR § 1.116 were considered, but did not place the application in condition for allowance. Appellants filed a Notice of Appeal on April 4, 2003.

Accordingly, the claims enclosed herein as Appendix A reflect the originally filed claims 1-20.

SUMMARY OF INVENTION

The present invention relates to a method of fabricating a thin film transistor including an organic gate-insulating layer having an improved interface property.

In another aspect, the invention relates to an apparatus for fabricating a thin film transistor, wherein the thin film transistor includes an organic insulating layer and an active

layer having a first amorphous silicon layer and a doped amorphous silicon layer over a substrate.

In another aspect, the invention relates to an apparatus for fabricating a transistor, wherein the transistor includes an organic layer and a semiconductor layer.

ISSUES

The issue is whether the Examiner properly rejected claims 1-5 and 15-20 under 35 U.S.C. § 103(a) as being unpatentable over the related art shown in Figures 1-4 in view of Yamazaki et al. (U.S. Pat. No. 6,261,881).

GROUPING OF CLAIMS

For purposes of this appeal brief only, and without conceding the teachings of any prior art reference, the claims have been grouped as indicated below:

Group/Claim(s)

A. Independent claim 1 and its dependent claims 2-5; Independent claim 15 and its dependent claims 16-17; and Independent claim 18 and its dependent claims 19-20; and

B. Independent claims 6 and 9 and their dependent claims 7-8 and 10-14, respectively, which have been withdrawn from consideration.

In Section VIII below, Appellants have included arguments supporting the separate patentability of each claim group as required by M.P.E.P. § 1206.

ARGUMENTS

The Examiner improperly rejected claims 1-5 and 15-20 under 35 U.S.C. § 103(a) as being unpatentable over the Related Art illustrated in Figures 1-4 in view of Yamazaki et al.

Independent claim 1 is allowable over the Related Art of Figures 1-4 ("Related Art") and U.S. Patent No. 6,261,881 issued to Yamazaki et al. ("Yamazaki et al.") in that claim 1 recites a method of fabricating a thin film transistor combination of elements including, for example, "heating the substrate in the equipment under vacuum and curing the organic insulating layer; and forming a silicon layer on the organic insulating layer in the equipment without breaking the vacuum." As discussed below, the Related Art neither teaches nor suggests these features.

Independent claim 15 is allowable over the combination of the Related Art and Yamazaki et al. in that claim 15 recites a method of forming a thin film transistor including, for example, "curing the organic layer in a first chamber; transferring the substrate having the organic layer from the first chamber to a second chamber without exposing the substrate having the organic layer to oxygen atmosphere during transfer; forming an active layer on the organic layer in the second chamber." As discussed below, the Related Art neither teaches nor suggests these features.

Independent claim 18 is allowable over the combination of the Related Art and Yamazaki et al. in that claim 18 recites a method of making a liquid crystal display device having a first substrate and a second substrate including, among other features, "curing the organic layer in a first chamber; transferring the first substrate having the organic layer from

the first chamber to a second chamber without exposing the first substrate having the organic layer to oxygen atmosphere during transfer; forming an active layer on the organic layer in the second chamber." As discussed below, the Related Art neither teaches nor suggests these features.

According to M.P.E.P. § 2143, establishment of a *prima facie* case of obviousness requires at least that the references relied upon teach or suggest all the claim limitations. See also *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Appellants respectfully submit neither the Related Art nor Yamazaki et al., analyzed alone or in any combination, teach or suggest all the claimed limitations of the present application. As presented above, the Related Art and Yamazaki et al. fail to teach or suggest a method of fabricating a thin film transistor that includes among other features: "...curing the organic insulating layer; and forming a silicon layer on the organic insulating layer in the equipment without breaking the vacuum", as recited in claim 1, and "curing the organic layer in a first chamber" and "forming an active layer on the organic layer in the second chamber", as recited in claims 15 and 18.

In the Related Art, benzocyclobutene (BCB) is deposited on a substrate having a gate electrode to form a BCB gate-insulating layer. Since BCB remains liquid under atmospheric conditions, the BCB must be cured after being deposited. Curing of BCB is usually performed under a nitrogen gas (N_2) in a heated oven. Because nitrogen gas is an inert gas, the nitrogen gas atmosphere (N_2) prevents the BCB from combining with oxygen gas (O_2). After curing, an active layer is formed in vacuum equipment. During this process of forming the BCB gate-insulating layer, the substrate having the BCB film remains in an atmospheric

condition during the transfer from the heated oven to the vacuum equipment. While exposed to this condition, atmospheric oxygen gas may combine with the surface of the BCB film, or contaminants in the atmosphere may be attached to the surface such that the BCB film is contaminated. If the BCB film has a contaminated surface, the interface property between the BCB gate-insulating layer and the active layer is deteriorated. If the interface is poor, then the electric characteristics of the thin film transistor deteriorate.

In rejecting claims 1-5 and 15-20 under 35 U.S.C. § 103(a), the Examiner states on page 4 of the final Office Action that Yamazaki et al. was not relied upon to teach "heating and curing the organic insulating layer under vacuum conditions…". In the Advisory Action, the Examiner further states that the purpose in citing Yamazaki et al. was that "the reference specifically teaches transporting the substrate from one stage to another in a highly vacuum state to prevent contamination of the surface of the substrate. And the combination of the teachings of Yamazaki et al. in the prior art would arrive to the claimed invention i.e., 'forming a silicon layer on the organic layer without breaking the vacuum as recited in claim 1; and transferring the organic layer from a first chamber to a second chamber and forming an active layer on the organic layer in the second chamber without exposing the substrate having the organic layer to oxygen atmosphere during transfer in claims 15 and 18'" (Advisory Action, paper no. 11, page 2). Appellants respectfully submit Yamazaki et al. teaches a method of making a liquid crystal display device and thin film transistor that is different from the invention as recited by the present claims. For example, in embodiment 3 and FIG. 5 of Yamazaki et al.:

> "a plastic substrate is formed as a substrate 500, a silicon oxide nitride (expressed as SiO_xN_y) film is formed as a base film 501

> and a tantalum film is formed as a gate wiring 502. Next, a BCB (benzocyclobutene) film with a thickness of 100 nm to 1 μm (preferably 500 to 800 nm) is formed as the first insulating film 503. At this step, the film thickness need to be thick enough to completely flatten the level difference due to the gate wiring 502. Having a great effect in flattening BCB film of not so thick a film thickness may sufficiently flatten the difference. After formation of the first insulating film 503, a second insulating film (silicon nitride oxide film) 504, an initial semiconductor film (microcrystalline silicon film) and an insulating film (silicon nitride oxide film) for serving as a protective film 509 are sequentially formed and layered without exposing them to the air. The microcrystalline film is formed at a formation temperature of 80 to 300 °C, preferably 140-200 °C, using as reaction gas silane gas diluted with hydrogen (SiH_4: H_2 = 1:10 to 100), setting the gas pressure to 0.1 to 10 Torr and setting the electric discharge power to 10 to 300 mW/cm^2. When used as the initial semiconductor film, the microcrystalline silicon film that has low hydrogen concentration within the film makes it possible to omit a heat treatment for reducing the hydrogen concentration. This embodiment prepares a chamber dedicated for formation of the second insulating film, a chamber dedicated for formation of the initial semiconductor film and a chamber dedicated for formation of the protective film to serially form those films by transferring the substrate from one chamber to another while keeping highly vacuumed state. The insulating films and the semiconductor film thus serially formed are all flat as they are formed on the flat surface." (Col. 15, lines 10-43)."

Based upon the above, Appellants respectfully submit the interface that Yamazaki et al. is concerned with is the interface between the second gate insulating layer and the semiconductor layer described in embodiment 3, not the interface between the first gate insulating layer (BCB) and the second insulating layer (SIN_x or SIO_2). As such, Yamazaki et al. fails to teach "curing the organic insulating layer" and "forming a silicon layer on the organic insulating layer in the equipment without breaking the vacuum", as recited in the claim 1, and "curing the organic layer in a first chamber" and "forming an active layer on the

organic layer in the second chamber", as recited in claims 15 and 18 of the present application. Thus, Yamazaki et al. fails to remedy the deficient teachings of the Related Art.

Because the Related Art and Yamazaki et al. fail to teach or suggest each of the features recited in the claims of the present application, no combination of the Related Art and Yamazaki et al. would provide a method having all the features recited in independent claims 1, 15 and 18 and their dependent claims 2-5, 16-17, and 19-20, respectively.

Appellants respectfully submit the Examiner has failed to establish a *prima facie* case of obviousness with regards to claims 1-5 and 15-20 and therefore, the rejection should be withdrawn and claims 1-5 and 15-20 allowed.

IX. CLAIMS INVOLVED IN THE APPEAL

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

Dated: October 3, 2003

Respectfully submitted,

By____________________

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 09/855,694

1. (Original) A method of fabricating a thin film transistor, the method comprising:

forming a gate electrode of the thin film transistor on a substrate;

depositing an organic insulating layer over the substrate having the gate electrode;

transferring the substrate to a heating and deposition equipment;

heating the substrate in the equipment under vacuum and curing the organic insulating layer; and

forming a silicon layer on the organic insulating layer in the equipment without breaking the vacuum.

2. (Original) The method of claim 1, wherein the organic insulating layer is selected from a group consisting of benzocyclobutene (BCB) and acryl.

3. (Original) The method of claim 1, wherein heating is performed under an inert gas condition.

4. (Original) The method of claim 3, wherein the inert gas includes nitrogen gas (N_2).

5. (Original) The method of claim 1, further comprising transferring the substrate from a first chamber of the equipment where the heating and curing take place to a second chamber of the equipment where the silicon layer is formed without breaking the vacuum.

6. (Withdrawn) An apparatus for fabricating a thin film transistor, wherein the thin film transistor includes an organic insulating layer and an active layer having a first amorphous silicon layer and a doped amorphous silicon layer over a substrate, the apparatus comprising:

a first reaction chamber for curing the organic insulating layer;

a second reaction chamber for forming the first amorphous silicon layer;

a third reaction chamber for forming the doped amorphous silicon layer; and

a preparation chamber for providing a vacuum condition,

wherein the preparation chamber is adjacent the first, second and third reaction chambers and the substrate is transferred from the first chamber to the second chamber under the vacuum condition through the preparation chamber.

7. (Withdrawn) The apparatus of claim 6, wherein the first reaction chamber is capable of introducing inert gas for curing.

8. (Withdrawn) The apparatus of claim 7, wherein the inert gas includes nitrogen gas (N_2).

9. (Withdrawn) An apparatus for fabricating a transistor, wherein the transistor includes an organic layer and a semiconductor layer, the apparatus comprising:

a first chamber for curing the organic layer;

a second chamber for forming the semiconductor layer; and

a preparation chamber adjacent the first and second chambers,

wherein the preparation chamber allows a product being formed into the transistor to transfer between the first and second chambers under vacuum.

10. (Withdrawn) The apparatus for fabricating a transistor according to claim 9, wherein the first chamber heats and cures the organic layer and the second chamber forms the semiconductor layer including amorphous silicon.

11. (Withdrawn) The apparatus for fabricating a transistor according to claim 9, wherein the first, second and preparation chambers are all in one unit.

12. (Withdrawn) The apparatus for fabricating a transistor according to claim 9, further comprising a third chamber for forming a second semiconductor layer, the preparation chamber allowing the product being formed into the transistor transfer from the second chamber to the third chamber under vacuum.

13. (Withdrawn) The apparatus for fabricating a transistor according to claim 9, wherein the first, second, third and preparation chambers are all in one unit.

14. (Withdrawn) The apparatus for fabricating a transistor according to claim 9, wherein the first chamber is capable of introducing inert gas during curing of the organic layer.

15. (Original) A method of forming a thin film transistor comprising:

forming a gate electrode on a substrate;

forming an organic layer over the substrate having the gate electrode;

curing the organic layer in a first chamber;

transferring the substrate having the organic layer from the first chamber to a second chamber without exposing the substrate having the organic layer to oxygen atmosphere during transfer;

forming an active layer on the organic layer in the second chamber; and

forming source and drain electrodes on the active layer.

16. (Original) The method of claim 15, further wherein the active layer includes an amorphous silicon layer and a doped amorphous silicon layer.

17. (Original) The method of claim 15, wherein the organic layer is cured under an inert gas atmosphere.

18. (Original) A method of making a liquid crystal display device having a first substrate and a second substrate, the method comprising:

forming a gate electrode on the first substrate;

forming an organic layer over the first substrate having the gate electrode;

curing the organic layer in a first chamber;

transferring the first substrate having the organic layer from the first chamber to a second chamber without exposing the first substrate having the organic layer to oxygen atmosphere during transfer;

forming an active layer on the organic layer in the second chamber;

forming source and drain electrodes on the active layer;

forming a pixel electrode connected to the drain electrode; and

forming a liquid crystal layer between the first substrate and the second substrate.

19. (Original) The method of claim 18, further wherein the active layer includes an amorphous silicon layer and a doped amorphous silicon layer.

20. (Original) The method of claim 18, wherein the organic layer is cured under an inert gas atmosphere.